Docket No.: I4303.0076
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:
Ravi Subramanian

Application No.: 09/772,584 — Confirmation No.: 2348

Filed: January 29, 2001 — Art Unit: 2182

For: A WIRELESS SPREAD SPECTRUM COMMUNICATION PLATFORM USING DYNAMICALLY RECONFIGURABLE LOGIC — Examiner: I. Park

**AMENDED**
**APPELLANTS' BRIEF ON APPEAL UNDER 37 C.F.R. § 1.192**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notification of Non-Compliant Appeal Brief dated November 13, 2006, Appellant submits this Amended Appellants' Brief on Appeal under 37 C.F.R. § 1.192.

In accordance with the provisions of 37 C.F.R. § 1.192, Appellant submits the following:



## I. REAL PARTY IN INTEREST

Based on information supplied by Appellant and to the best of the Appellant's legal representative's knowledge, the real party of interest is the assignee, Infineon Technologies AG.

## II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no related appeals, interferences, or judicial proceedings which might directly affect or be directly affected by or have a bearing on the Board's decision in the pending Appeal.

III. STATUS OF CLAIMS

Pursuant to the final Office Action dated November 5, 2004, claims 1-16 and 51-66 remain rejected under 35 U.S.C. § 102(e) as being anticipated by Sharrit et al. (U.S. Patent No. 5, 999,990). Claims 17-50 and 67-98 are withdrawn from consideration. Thus, claims 1-98 are pending in the application, with claims 1-16 and 51-66 on appeal.

IV. STATUS OF AMENDMENTS

A Response was filed on May 5, 2005, after the Final Rejection; amendments to the claims were presented. The Response was entered, as indicated in the May 31, 2005 Advisory Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a processor *[102a]* having a plurality of kernel planes *[201a-201i]* with a plurality of kernels *[261a-266a]* for processing data in a communication device. *[See page 25, lines 26-27, and Fig. 2C.]* At least one kernel *[261a]* of the plurality of kernels *[261a-266a]* includes an interface *[278]* adapted to receive and transmit information from the at least one kernel *[261a]*. *[See page 28, lines 27-34, and Fig. 2D.]* A satellite kernel *[270]* is coupled to the interface *[278]*, wherein the satellite kernel *[270]* performs a discrete class of operations within a communications application. *[See*

*page 4, lines 18-19, page 30, lines 22-28, page 32, lines 15-16, and page 61, lines 17-19, and Figs. 2C and 2D.]* A local controller *[271]* is coupled to the interface and the satellite kernel *[270]*, the local controller *[271]* permitting the at least one kernel *[261a]* to operate autonomously with respect to the other of the plurality of kernels *[262a-266a]* in the respective kernel plane *[201]*. *[See page 30, line 7 through page 31, line 3, page 53, lines 28-32, page 64, lines 16-25, Figs. 2C-E, and inherent.]*

Independent claim 51 is directed to a computer readable medium *[Appendices A and B, page 54, lines 9-27, and page 63, line 7 through page 64, line 25]* containing therein computer readable codes that enable an electronic device to access at least one kernel architecture of a plurality of kernel architectures *[261a-266a]* in one of a plurality of kernel plane architectures *[201a-201i]*. *[See page 25, lines 26-27, and Fig. 2C.]* The method performed by the computer readable medium includes reading an interface architecture *[278]*, the interface architecture adapted to receive and transmit information from the at least one kernel architecture *[261a]*. *[See page 28, lines 27-34, and Fig. 2D.]* A satellite kernel architecture *[270]* is read and is coupled to the interface architecture *[278]*, the satellite kernel architecture *[270]* performing a discrete class of operations within a communications application. *[See page 4, lines 18-19, page 30, lines 22-28, page 32, lines 15-16, and page 61, lines 17-19, and Figs. 2C and 2D.]* A local controller architecture *[271]* is read, the

local controller architecture being coupled to the interface architecture *[278]* and the satellite kernel architecture *[270]*, the local kernel architecture *[271]* permitting the at least one kernel architecture *[261a]* to operate autonomously with respect to other of the plurality of kernel architectures *[262a-266a]*. *[See page 30, line 7 through page 31, line 3, page 53, lines 28-32, page 64, lines 16-25, Figs. 2C-E, and inherent.]*

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-16 and 51-66 were erroneously rejected under 35 U.S.C. § 102(e) as being anticipated by Sharrit et al. (U.S. Patent No. 5, 999,990).

## VII. ARGUMENT

Sharrit et al. is directed to a communicator 10, which includes a plurality of reconfigurable resource units (RRUs) 13, a signal bus 14, a controller 16, etc. The plurality of RRUs 12 can each be dynamically altered to perform any of a plurality of processing tasks. The controller 16 determines a plurality of processing tasks to be supported by the communicator and configures the plurality of RRUs 12 accordingly.

As illustrated in Fig. 3 of Sharrit, an RRU 54 can include a general purpose processor (GPP) 48 and a field programmable gate array (FPGA) 50. To configure the FPGA 50, the GPP 48 delivers a configuration file to an input of the FPGA 50. The GPP 48

is coupled to the controller 16 for receiving instructions on how to process a signal on bus 14. In response to the instructions, the GPP 48 delivers a control signal to FPGA 50 instructing it to read the signal on signal bus 14 and to process the signal in an appropriate area of the cell array.

Alternatively, as illustrated in Fig. 4 of Sharrit, an RRU 58 can include both hardware and software programmability. That is, RRU 58 includes a GPP 60, an FPGA 62, a DSP 64 with associated RAM 66, and a multiplexer 68. RRU 58 is a hybrid unit which allows controller 16 to specify whether a signal currently on signal bus 14 will be processed in hardware (in FPGA 62) or in software (in DSP 64). Based on commands from controller 16, GPP 60 delivers a select signal to multiplexer 68 that directs the signal on bus 14 to the desired processing unit. Also, as indicated by the arrows, the GPP 60 configures the FPGA 62 or the DSP 64 to run certain software modules.

Sharrit does not teach, or even suggest, a kernel having a local controller that permits the kernel to operate autonomously with respect to other of a plurality of kernels, as required by the claimed invention. Sharrit has centralized control in its controller 16 as opposed to the claimed distributed control. Sharrit's controller 16 MIPS rating and bus 14 width and speed ratings limit the number of RRU's or the reconfiguration abilities versus time. With equal ratings for the controller and buses, the distributed control system of the

claimed invention is more scaleable in that it can support more kernels or more reconfigurations per second than Sharrit.

Contrary to the Examiner's statement on page 3 of the final Office Action, Sharrit's GPP (general purpose computer), which operates in conjunction with a FPGA (Fig. 3) or a FPGA and DSP (Fig. 4), is not equivalent to the claimed local controller. There is no suggestion in Sharrit that the GPP performs local controller functions. All control must be centralized in the controller 16. In order for the GPP to perform local controller functions and do resource allocation, it would need to obtain information from the DSP and/or FPGA. Since information is transmitted only from the GPP to the DSP and/or the FPGA and not the reverse (as indicated by the single-headed arrow), the GPP can not know how loaded the DSP is. Only through the local controller 16 can the GPP know this information.

Further, the Sharrit system does not scale well as the number of RRU increases. The performance of the single controller 16 and bus 14 places a limit on the maximum number of RRUs. For example, assume Sharrit has one chip with 4 RRUs and another chip with 8 RRUs. If Sharrit then requires a chip with 16 RRUs, the single controller 16 and bus 14 must be redesigned for higher performance (which may not even be possible). Thus Sharrit does not have good scalability.

On the other hand, the claimed kernel's local controller scales wells as the number of kernels increases. In a system with distributed control, the performance of the local controllers in the respective kernels do not increase as a function of total kernels. That is, the individual kernels do not increase in complexity as the network grows. All kernels simply run the same protocol, and as the network grows kernels may experience longer latencies. If the application can tolerate increased or unknown latency, then the local controllers may not need to increase in complexity. By way of analogy, a computer connected to an IP network does not require the individual computers to increase in complexity and performance as the number of networked computers increases.

In view of the above remarks, it is respectfully submitted that claims 1-16 and 51-66 are patentable over Sharrit. Reconsideration and withdrawal of this rejection is therefore respectfully requested.

VIII. <u>CLAIMS</u>

A copy of the claims involved in the present appeal is attached hereto as Claims Appendix.

## IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

## X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above.

Please charge any fee, except for the Issue Fee, that may be necessary for the continued pendency of this application to our Deposit Account No. 04-0100.

Dated: December 13, 2006

Respectfully submitted,

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## CLAIMS APPENDIX

**CLAIMS 1-16 AND 51-66 ARE ON APPEAL:**

1. In a processor having a plurality of kernel planes with a plurality of kernels for processing data in a communication device, at least one kernel of the plurality of kernels comprising:

an interface adapted to receive and transmit information from the at least one kernel;

a satellite kernel coupled to the interface, the satellite kernel performing a discrete class of operations within a communications application; and

a local controller coupled to the interface and the satellite kernel, and the local controller permitting the at least one kernel to operate autonomously with respect to the other of the plurality of kernels.

2. The processor recited in claim 1 wherein the satellite kernel is configurable to perform a specific sub function within the class of sub functions.

3. The processor recited in claim 1 wherein the satellite kernel is reconfigurable from a first sub function to perform a second sub function within the discrete class of operations.

4. The processor recited in claim 1 wherein the satellite kernel is reconfigurable only within the class of operations.

5. The processor recited in claim 1 wherein the satellite kernel includes a plurality of electronic devices for performing arithmetic, logic, and storage operations, the plurality of electronic devices coupled to each other and to the local controller in a fixed manner for implementing functions common to the class of operations, the plurality of electronic devices coupled to each other in a reconfigurable manner for implementing functions unique within the class of operations.

6. The processor recited in claim 5 wherein the electronic devices are coupled to each other using a reconfigurable logic technique, a reconfigurable datapath technique, a reconfigurable dataflow technique, or a reconfigurable control technique for the discrete class of operations performed by the satellite kernel.

7. The processor recited in claim 6 wherein the electronic devices are coupled to each other using a heterogeneous combination of the reconfigurable logic technique, the

reconfigurable datapath technique, the reconfigurable dataflow technique, or the reconfigurable control technique.

8. The processor recited in claim 4 wherein the reconfigurability of the at least one kernel is established on a temporal basis, a logical basis, or a functional basis.

9. The processor recited in claim 8, wherein the class of operations is based upon a desired level of performance for the application.

10. The processor recited in claim 1 wherein the discrete class of operations is an algorithm.

11. The processor recited in claim 1, wherein the class of operations is limited to a class of mathematical field operations.

12. The processor recited in claim 1, wherein the application within which the operations are used is a wireless communications application.

13. The processor recited in claim 12, wherein the operations used in the wireless communications application include modem operations and codec operations.

14. The processor recited in claim 1, wherein the local controller manages the satellite kernel autonomously from circuitry outside of the processor.

15. The processor recited in claim 1 wherein the satellite kernel includes a computing element at a lower hierarchical level than the satellite kernel.

16. The processor recited in claim 5 wherein the satellite kernel includes a plurality of selective interconnects coupling the plurality of electronic devices.

51. A computer readable medium containing therein computer readable codes that enable an electronic device to access at least one kernel architecture of a plurality of kernel architectures in one of a plurality of kernel plane architectures, the method comprising:

reading an interface architecture, the interface architecture adapted to receive and transmit information from the at least one kernel architecture;

reading a satellite kernel architecture, the satellite kernel architecture coupled to the interface architecture, the satellite kernel architecture performing a discrete class of operations within a communications application; and

reading a local controller architecture, the local controller architecture being coupled to the interface architecture and the satellite kernel architecture and permitting the at least one kernel architecture to operate autonomously with respect to other of the plurality of kernel architectures.

52. The computer readable medium recited in claim 51 wherein the satellite kernel architecture is configurable to perform a specific sub function within the class of sub functions.

53. The computer readable medium recited in claim 51 wherein the satellite kernel architecture is reconfigurable from a first sub function to perform a second sub function within the discrete class of operations.

54. The computer readable medium recited in claim 51 wherein the satellite kernel architecture is reconfigurable only within the class of operations.

55. The computer readable medium recited in claim 51 wherein the satellite kernel architecture includes a plurality of electronic devices for performing arithmetic, logic, and storage operations, the plurality of electronic devices coupled to each other and to the local controller architecture in a fixed manner for implementing functions common to the class of operations, the plurality of electronic devices coupled to each other in a reconfigurable manner for implementing functions unique within the class of operations.

56. The computer readable medium recited in claim 55 wherein the electronic devices are coupled to each other using a reconfigurable logic technique, a reconfigurable datapath technique, a reconfigurable dataflow technique, or a reconfigurable control technique for the discrete class of operations performed by the satellite kernel.

57. The computer readable medium recited in claim 56 wherein the electronic devices are coupled to each other using a heterogeneous combination of the reconfigurable logic technique, the reconfigurable datapath technique, the reconfigurable dataflow technique, or the reconfigurable control technique.

58. The computer readable medium recited in claim 54 wherein the reconfigurability of the at least one kernel architecture is established on a temporal basis, a logical basis, or a functional basis.

59. The computer readable medium recited in claim 51 wherein the class of operations is based upon a desired level of performance for the application.

60. The computer readable medium recited in claim 51 wherein the discrete class of operations is an algorithm.

61. The computer readable medium recited in claim 51 wherein the class of operations is limited to a class of mathematical field operations.

62. The computer readable medium recited in claim 51, wherein the application within which the operations are used is a wireless communications application.

63. The computer readable medium recited in claim 62, wherein the operations used in the wireless communications application include modem operations and codec operations.

64. The computer readable medium recited in claim 51, wherein the local controller architecture manages the satellite kernel architecture autonomously from circuitry outside of the electronic device.

65. The computer readable medium recited in claim 51 wherein the satellite kernel architecture includes a computing element architecture at a lower hierarchical level than the satellite kernel architecture.

66. The computer readable medium recited in claim 55 wherein the satellite kernel architecture includes a plurality of selective interconnects coupling the plurality of electronic devices.

# EVIDENCE APPENDIX

All evidence is in the record.

## RELATED PROCEEDINGS APPENDIX

There are no related proceedings for this matter.